ABSTRACT

This paper presents a novel super-pipelined VLSI architecture for Viterbi decoders. This architecture is capable of achieving high throughput in an area-efficient manner and hence it is an attractive architecture for implementing the Viterbi decoder where a large constraint length and high throughput rate are required. The throughput can be linearly increased by increasing the number of basic process element. The notable advantage is its regularity and flexibility. A Viterbi decode (R=1/2 K=10) is designed in 0.6um 3.3V CMOS process to demonstrate the favourable performance of this new architecture.

1. INTRODUCTION

With the development of digital communications, high speed large-constraint-length Viterbi decoders will be required to yield higher coding gain and provide large ability to transmit more data in the same channel. [1][2]

For high speed applications, parallel architectures are employed. Such parallel implementations consumes large silicon area. Placement and routing is a difficult task. [3][4][5]. For a large-constraint-length Viterbi decoder, state-sequential architectures are often utilized to realize the single-ship Viterbi decoder, where the silicon area can be effectively reduced. However, the throughput is very low.[6][7]Therefore, an efficient trade-off between area and speed has to be done in VLSI implementation of high speed large-constraint-length Viterbi decoders. To date, the pipelined architecture is one of the best choices for high throughput and large-constraint-length Viterbi decoders. A number of pipelined architectures have been proposed [8][9]. However, there is one drawback of pipelined architecture -- the highest speed is limited by the highest speed of ACS. When the speed of ACS unit is fixed, the speed of pipelined Viterbi decoder is also fixed. The parallel pipelined architecture [10]and systolic array architecture [11] have been developed to further increase the speed. But these architectures increase the control complexity significantly and they are not flexible for different throughput application.

In this paper, we presented a novel super-pipelined architecture which linearly increases the speed by increasing the number of process elements with slightly increasing the control complexity. In this architecture, the basic process elements (PE) are pipelined and each basic process element (PE) has \(v-1\) identical pipelined sub-process-elements (PE\(i\), \(i=1, 2, ..., v-1\)), where \(v\) is the constraint length. The one advantage of this architecture is its ability of achieving high throughput in an area-efficient manner and hence it is an attractive architecture for implementing the Viterbi decoder where a large constraint length and high throughput rate are required. The other notable advantage is its linearly increasing the speed with slightly increasing the control complexity. Meantime, regularity and flexibility feature another advantage of this new architecture which can be easily implemented in VLSI. Based on this new architecture, Viterbi decode (R=1/2 K=10) is designed in 0.6um 3.3V triple-metal CMOS process to demonstrate the favourable performance of proposed new architecture.

2. VITERBI ALGORITHM

Viterbi algorithm is based on dynamic programming computations[12]. Its data flow can be expressed by a trellis graph. The vertices of trellis are called states and associated numerical values path metric \(pm\). When the constraint length is \(v\), the trellis graph contains \(2^{v-1}\) states at any given time. Edge weights are given by the branch metric \(bm\). One of the major steps in the Viterbi algorithm is to update the path metrics according to the following equations(1)(2):

\[
\begin{align*}
pm_{i'}, t + 1 & = \min(pm_{k}, t + bm_{i'i'}, pm_{j'}, t + bm_{jj'}) \\
& \quad \text{where } i', j' \\
\end{align*}
\]

(1)

\[
\begin{align*}
pm_{j'}, t + 1 & = \min(pm_{i}, t + bm_{ij'}, pm_{j'}, t + bm_{jj'}) \\
& \quad \text{where } i, j \\
\end{align*}
\]

(2)

Figure 1. shows this updating process. Every new path metric is the lesser of two sums, which is old path metric plus its corresponding branch metric. So we call it add, compare and select (ACS) process.
The traditional trellis graph has identical geometry, which can be easily realized in state-parallel architecture. There is another alternative form of the trellis graph depicted in figure 2. (assumed the constraint length is 5), which shows one cycle of in-place computation of Viterbi decoder. Each cycle includes \( v-1 \) stages computation, where \( v \) is constraint length. It is a unique property of Viterbi algorithm that the state order will be in natural order after one full cycle. That means the output of the previous cycle can be directly connected to the input of next cycle without recirculation.

3. ARCHITECTURE

3.1. Single-path delay feedback pipelined architecture

The pipelined architecture is the best choice for high throughputs and area-efficient applications due to its regular structure and relatively simple control. Figure 3. shows Single-path delay feedback (SDF) pipelined architecture for a viterbi decoder with constraint length 10. When \( v = 10 \), the full cycle of computation contains \( v-1=9 \) pipelined stages. We call this full cycle one Process Element (PE). One PE has \( v-1 \) identical sub-process-elements (PE\(_i\), \( i=1,2...v-1 \)). PE\(_i\) is the \( i \)th sub-process-element in one full cycle. The data is processed between stages in a single path and feedback is used to store new inputs and intermediate results. The basic idea behind this scheme is to accept the scrambling of data in memories, and to adapt and unscramble, and then the next stage can receive the correct data. When the FIFOs are filling with the first half of inputs, the last half of results are been shifting out. During this time, the operational elements should be bypass. When the first half of inputs are shifting out of the FIFOs, the second half of inputs are shifting into the process element and the second half of results are filling the FIFOs. During this time, the operational elements are working. In figure 3., each PE\(_i\) (sub process element) includes four adders and two comparators and four multiplexer.

Although the pipelined architecture significantly increase the throughput compared with state-sequential architecture, there is one main drawback --the throughput is still limited by the highest speed of ACS. The super-pipelined
architecture is proposed to resolve this shortcoming and achieve higher throughput.

3.2 Super-pipelined viterbi architecture

PE (one full in-place computation cycle) is the basic unit of the Viterbi decoder. Inside each PE, the pipelined architecture has been used to cascade the sub-process-element. Figure 4. shows the simplified SDF pipelined architecture for Viterbi decoders (constraint length is 10) where only one computation cycle (PE) is utilized. In order to further increase the speed, the PE can be further cascaded and pipelined which is called “super-pipelined architecture”. Figure 5. shows this super-pipelined architecture where N process elements (PE) are pipelined. The speed will be linearly increased by the factor of N (the number of PE). Meanwhile this architecture do not increase the control complexity significantly which can be efficiently implemented in VLSI. It is flexible to select N (number of process elements) for different throughput requirement.

Assumed the speed of traceback is high enough to match the speed of ACS, we summary the speed and area of several architectures in figure 6(a) and (b) where we let the highest speed of ACS be 1 and the area of each ACS be 1. From the curves, we have such conclusions: the full parallel architecture is suitable for high speed small-constraint-length Viterbi decoders; The state-sequential architecture is for low speed large-constraint-length applications; The SDF pipelined architecture can be used to realize moderate-speed large-constraint length Viterbi decoders. The SDF super-pipelined architecture is the best trade-off between speed and area and hence can be employed in the design of high speed large-constraint length Viterbi decoders.

4. IMPLEMENTATION

To demonstrate the advantage of the SDF super-pipelined architecture presented in this paper, we design a viterbi
decoder with convolutional code rate 1/2 and constraint length 10 in 0.6um CMOS process. Each of ACS units in our design can be clocked at 70 MHz. An efficient traceback method [13] [14] has been used to speed up the traceback circuit. Let N be 2 (the number of PE) and each PE includes 9 sub-PEs. It can work at the maximum data-rate of 2.4Mb/s. The core size is about 40 mm². The floorplan is shown in figure 7 and figure 8 shows the layout of a sub-process-element (PEi) which is compiled by Compass data-path compiler.

5. CONCLUSIONS

The primary task of this paper is to present an efficient VLSI architecture for high throughput large-constraint-length Viterbi decoder. This architecture is capable of achieving high throughput in an area-efficient manner and hence it is an attractive architecture for implementing the Viterbi decoder where a large constraint length and high throughput rate are required. The architecture linearly increase the speed by the factor of N (number of process element) with slightly increasing control complexity. Meanwhile it can achieve different throughput requirement by selecting the parameter N. Its regularity and flexibility make it easily implemented in VLSI.

6. ACKNOWLEDGMENT

This work is financially supported by Foundation for Strategic Research in Sweden.

7. REFERENCES


Figure 7. Floorplan of Viterbi decoder (constraint length 10).

Figure 8. Layout of one sub-process-element