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Design and Process Issues of Junction- and Ferroelectric- Field Effect Transistors in Silicon Carbide

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AKADEMISK AVHANDLING

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Abstract

In today's solid-state electronics, Si and SiO_2 are the dominant materials used. However, new materials such as SiC or ferroelectrics are required for some special applications since superior characteristics can be achieved in electronic devices. The main objective of this work is the design, fabrication and characterization of different field effect transistors (FETs) including the new device structures referred to as junction-gated metal-oxide-semiconductor FET (JMOSFET) and ferroelectric-FET (FeFET) as well as the conventional junction-FET (JFET).

Buried-gate JFETs with two different structures have been fabricated in epitaxial layers of 4H-SiC using only 2- to 3-mask steps. It has been shown that the trenching effect during dry etching can induce static induction transistor (SIT)-like drain conduction for JFETs with small channel thickness (less than 0.5 micro-meter). The conduction mechanism in these JFETs is examined by the potential profiles from two-dimensional numerical simulations. The trenching effect can be reduced for JFETs using an oxide mask for dry etching with sloped etch profile (an angle of around 30°). It has also been demonstrated that, by introducing a sacrificial oxidation (SO) step on the inductively coupled plasma (ICP)-etched surface of SiC, the electrical properties of MOS capacitors and Ohmic contacts can be effectively recovered after dry etch damage. The switching performance of JFETs in a test circuit has been investigated with an inductive load and compared with numerical device simulations. A drain voltage rise/fall time of around 30 ns has been observed for turn-off and turn-on. The results have been compared to numerical mixed-mode circuit simulations with finite element structures.

To improve the high temperature stability and to lower the on-state resistance, we have designed the so-called 'JMOSFET', which is a buried-gate JFET with an additional MOS-gate on top. The JMOSFETs have shown the feasibility for operation with a constant current level from room temperature all the way up to 300 ^oC by applying proper backside-gate voltage. An advantage of this device is the improved channel transconductance (2.5 times), which results from accumulating the *n*-channel with the MOS gate.

In realizing ferroelectric devices above room temperature and in severe environment, high temperature polarization behavior and retention of ferroelectric thin films are critical factors to explore. Thus SiC is one of the most attractive semiconductor material for these applications. We have found an optimum ferroelectric gate structure (using pulsed laser deposition) of PZT/Al_2O_3/4H-SiC (large *C-V* memory window of 10 V, low conductance <0.1 mS/cm^2, tangent delta of 0.0007 at 400kHz). Based on this structure, the nonvolatile operation of FeFETs in SiC has been shown for the first time at elevated temperatures. The transistor showed a memory effect from room temperature up to 200 ^oC and stable transistor operation was observed up to 300 ^oC. The retention of the nonvolatile memory was 2×10^4 seconds at 150 ^oC without applying bias on the gate.

Keywords: silicon carbide, ferroelectrics, PZT, field effect transistor, FET, JFET, MOSFET, device simulation, capacitance-voltage measurements, pulsed laser deposition